Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of testing a clock and data recovery device (CDR), comprising:

producing test data from a first CDR; ~~and~~

~~testing another second CDR based on the test data from the first CDR;~~

outputting the test data based on a clock;

generating data drift in the test data by changing a phase of the clock;

setting the phase of the clock based on a count value;

changing the count value across a range of phase shifts;

incrementing/decrementing the count value until a maximum/minimum count value is reached;

subsequently decrementing/incrementing the count value until a minimum/maximum count value is reached; ~~and~~

repeating the incrementing/decrementing step and the subsequently decrementing/incrementing step ~~above steps~~ until all the test data is generated; and

testing a second CDR based on the test data from the first CDR.

2-4. (Canceled)

5. (Withdrawn) The method of claim 1, further comprising:

adding one or more least significant bits to the counter value;

incrementing/decrementing added least significant bits when incrementing/decrementing the counter value.

6. (Withdrawn) The method of claim 1, further comprising:

generating test data results in the second CDR device; and

verifying the test data results.

7. (Withdrawn) The method of claim 1, further comprising:

producing test data from the second CDR; and

testing the first CDR based on the test data from the second CDR.

8-9. (Canceled)

10. (Previously Presented) A clock and data recovery device (CDR), comprising:

a phase variable clock source to generate a phase variable clock;

a test data generator to generate test data based on the phase variable clock;

a counter that has a count value to control a phase of the phase variable clock; and

a finite state machine to increment/decrement the count value until a maximum/minimum count value is reached, and subsequently decrement/increment the count value until a minimum/maximum count value is reached,

wherein the finite machine increments/decrements the count value until all the test data is generated.

11. (Canceled)

12. (Withdrawn) The CDR of claim 10, wherein:

the counter includes one or more least significant bits added to the counter value, the counter without the least significant bits are used to control the phase of the phase variable clock; and

the finite state machine increments/decrements the least significant value bits when incrementing/decrementing the counter value.

13. (Original) The CDR of claim 10, wherein the test data generator is a pseudo random number generator.

14. (Original) The CDR of claim 10, wherein the phase variable clock source is a phase rotator coupled to a phase locked loop (PLL) oscillator.

15. (Original) A system or a network implementing the CDR of claim 10.

16. (Previously Presented) A clock and data recovery device (CDR) to test another second CDR, comprising:

means for generating test data to test the second CDR;

means for producing a range of data drift conditions in the test data by changing a phase of a clock;

means for setting the phase of the clock based on a count value;

means for changing the count value across a range of phase shifts;

means for incrementing/decrementing the count value until a maximum/minimum count value is reached, and subsequently decrementing/incrementing the count value until a minimum/maximum count value is reached.

17. (Original) The CDR of claim 16, wherein means for producing a range of data drift conditions include means for reducing a rate of data drift.

18. (Previously Presented) An apparatus including a plurality of clock and data recovery devices, comprising:

a first CDR having a test data generator and a finite state machine to adjust data drift in the test data by setting a phase of a clock based on a count value; and

another second CDR, wherein the first CDR uses the test data generator to generate test data to test the second CDR,

wherein the finite state machine increments/decrements the count value until a maximum/minimum count value is reached, and subsequently decrements/increments the count value until a minimum/maximum count value is reached, and

wherein the finite machine increments/decrements the count value until all the test data is generated.

19. (Canceled)

20. (Withdrawn) The apparatus of claim 18, further comprising:

the second CDR having a data checker to check a test data result output.